Rakshith Saligram

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Education

2019 – Present
Georgia Institute of Technology, Atlanta, Georgia
PhD, School of Electrical and Computer Engineering
Advisor: Arijit Raychowdhury

2014 – 2016
University of Southern California, Los Angeles, California
M.S. Honors, Ming Hsieh Department of Electrical Engineering
Major: VLSI Design and Computer Engineering

2009 – 2013
BMS College of Engineering, Bangalore, Karnataka
B.E. Electronics and Communication Engineering
Thesis: Design of Fault Tolerant ALU using Parity Preserving Reversible Logic Gates

Academic & Research Experience

2019 – Present
Integrated Circuits and Systems Research Lab
Graduate Research Assistant
Area of Interest: Cryogenic CMOS Circuits, VLSI, Thermal Analysis, High Speed IO Design

* *DARPA LTLT*: Model, Design, Analyze & Tapeout Dense Cryogenic Memories.
* *DARPA THERMONAT*: Model & Analyze Self Heating in Advanced Logic Devices.
* *Microsoft HPC*: Cryogenic CMOS for High Performance Computing in Servers.
* *Samsung-GRO*: Compact Modeling of Cryogenic CMOS Devices and Interconnects.
* *ASCENT*: Higher Order Modulation techniques for inter-Chiplet Communication.

Fall 2015
USC Ming Hsieh Institute - Department of Electrical Engineering
Course Development Assistant
Assist the Department Chair of EE Systems to develop and improve EE477L (MOS VLSI Circuit Design) course curriculum.

Summer 2015
USC Ming Hsieh Institute - Department of Electrical Engineering
Course Grader Modern Solid-State Devices
Provide solutions and grade the assignments for EE537- Modern Solid-State Devices course and hold office hours for discussion.

2013 – 2014
Department of ECE, BMS College of Engineering
Lecturer

* Instructed freshmen, sophomore & junior classes and senior lab. Visit my homepage for details about the classes.
* Functioned as department coordinator for National Board of Accreditation (NBA).

Industry Experience

Summer/Fall 2022 — **IMEC USA Nanoelectronic Design Center Inc.**
Superconducting Research Intern
Worked on high speed comparators and pre-amplifiers for superconductor-CMOS interface circuits at 77K and Noise Modelling for cryogenic channels

Summer 2020 — **ARM Inc.**
Intern Research
Worked on benchmarking ARM cores at cryogenic Temperatures, Recharacterization of standard cells at lowered Vdd and iso-performance, self heating analysis

2016-2018 — **Intel Corporation**
Graphics Hardware Engineer in Dual Sub-Slice Marco (DSSM)
Resposible for RTL to GDS-II of multiple generations of Intel's GFx Processors. Worked on timing analysis, timing and routing closure, ECO, Performance verification at block, partition, section, slice and full-chip levels

Research Publications

Journal Articles

1. Gaidhane, A. D., **Saligram**, **R.**, Chakraborty, W., Datta, S., Raychowdhury, A., & Cao, Y. (2023). Predictive Modeling and Benchmarking of Cryogenic FinFETs for Energy-Efficient Computing (under review). *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*.
2. **Saligram**, **R.**, Raychowdhury, A., & Datta, S. (2023). The Future is Frozen: Cryogenic CMOS for High Performance Computing (under review). *(Invited) Elsevier Chip*.
3. **Saligram**, **R.**, Datta, S., & Raychowdhury, A. (2022). Design Space Exploration of Interconnect Materials for Cryogenic Operation: Electrical and Thermal Analyses. *IEEE Transactions on Circuits and Systems - I: Regular Papers, (TCAS-I)*.
4. **Saligram**, **R.**, Chakraborty, W., Cao, N., Cao, Y., Datta, S., & Raychowdhury, A. (2021). Power Performance Analysis of Digital Standard Cells for 28nm Bulk CMOS at Cryogenic Temperature using BSIM models. *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*.
5. Wriddhi, C., Aabrar, K. A., Gomez, J., **Saligram**, **R.**, Raychowdhury, A., & Datta, S. (2021). Characterization and Modeling of 22nm FDSOI Cryogenic RF CMOS. *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*.
6. **Saligram**, **R.**, Datta, S., & Raychowdhury, A. (2021a). Cryomem: A 4K-300K 1.3Ghz Hybrid 2T-Gain-Cell based eDRAM Macro in 28nm Logic Process for Cryogenic Applications. *(Invited), IEEE Solid State Circuit Letters*, *4*.
7. **Saligram**, **R.**, Datta, S., & Raychowdhury, A. (2021b). Scaled Back End of Line Interconnects at Cryogenic Temperatures. *IEEE Electron Device Letters*, *42*(11).
8. Bairy, B., Craig, T. S., Gonde, K., Gupta, N., Prajogi, A., Wilner, M., & **Saligram**, **R.** (2016b). Mitigating the impact of NBTI and PBTI Degradation. *Global Journal of Technology and Optimization*, *7*, 195.
9. **Saligram**, **R.**, Hegde, S., Kulkarni, S., Bhagyalakshmi, H., & Venkatesha, M. (2013a). Design of Parity Preserving Logic Based Fault Tolerant Reversible Arithmetic Logic Unit. *International Journal of VLSI Design and Communication Systems*, *10*.
10. **Saligram**, **R.**, Hegde, S., Kulkarni, S., Bhagyalakshmi, H., & Venkatesha, M. (2013b). Design of Fault Tolerant Reversible Multiplexer Based Multi-Boolean Function Generator using Parity Preserving Gates. *International Journal of Computer Applications*.

11. **Saligram**, **R.**, & Ravishankar, R. (2012). Novel Code Converter Employing Reversible Lgic. *International Journal of Computer Applications*.

Conference Proceedings

1. Lakshminarasimhan, K., Ashby, T., **Saligram**, **R.**, Glass, J., Bhattacharjee, D., Evenblij, T., Perumkunnil, M., Mallik, A., & Herr, A. (2024). CRATER: Superconducting Customized Regular Arrays for Transformers (under review), In *International Symposium on Computer Architecture (ISCA) 2024*, Argentina, Buenos Aires.
2. Wang, W.-C., **Saligram**, **R.**, Sharma, S., Lee, M., Gaidhane, A., Cao, Y., Raychowdhury, A., Datta, S., & Mukhopadhyay, S. (2023). Cool-CIM: Cryogenic Operation of Analog Compute-In-Memory for Improved Power-Efficiency, In *IEEE International Electron Device Meeting (IEDM) 2023*, USA, San Francisco.
3. **Saligram**, **R.**, Datta, S., & Raychowdhury, A. (2023). Cryogenic CMOS as an Enabler for Low Power Dynamic Logic, In *ACM/IEEE International Symposium on Low Power Electronics and Design 2023*, Vienna, Austria.
4. Herr, A., **Saligram**, **R.**, Van-Winckel, S., Glass, J., Perumkunnil, M., Ashby, T., Brebels, S., Ravex, A., Banerjee, A., & Herr, Q. (2022). Dual Temperature Memory Hierarchy and High Speed High Density Data Links for Superconducting Digital Systems, In *Applied superconductivity conference 2022*, Hawaii, USA.
5. Chakraborty, W., Shreshta, P., Gupta, A., **Saligram**, **R.**, Spetalnick, S., Campbell, J., Raychowdhury, A., & Datta, S. (2022). Multi-bit per-cell 1T SiGe Floating Body RAM for Cache Memory in Cryogenic Computing, In *IEEE VLSI Technology Symposium (VLSI) 2022*, Hawaii, USA.
6. Chakraborty, W., **Saligram**, **R.**, Gupta, A., Jose, M. S., Aabrar, K. A., Dutta, S., Khanna, A., Raychowdhury, A., & Datta, S. (2021). Pseudo-Static 1T Capacitorless DRAM using 22nm FDSOI for Cryogenic Cache Memory, In *67th IEEE International Electron Device Meeting (IEDM) 2021*, San Francisco, USA.
7. Chakraborty, W., Aabrar, K. A., Gomez, J., **Saligram**, **R.**, Raychowdhury, A., & Datta, S. (2021). Cryogenic RF CMOS on 22nm FDSOI Platform with Record ft=495GHz and fMAX=497GHz, In *VLSI Technology Symposia, 2021*, Virtual, Japan.
8. **Saligram**, **R.**, Datta, S., & Raychowdhury, A. (2021c). Cryomem: A 4K-300K 1.3GHz eDRAM Macro with Hybrid 2T-Gain-Cell in a 28nm Logic Process for Cryogenic Applications, In *IEEE Custom Integrated Circuits Conference (CICC) 2021*, Virtual, USA.
9. **Saligram**, **R.**, Prasad, D., Pietromonaco, D., Raychowdhury, A., & Cline, B. (2021). A 64-Bit Arm CPU at Cryogenic temperatures: Design Technology Co-Optimization for Power and Performance, In *IEEE Custom Integrated Circuits Conference (CICC) 2021*, Virtual, USA.
10. **Saligram**, **R.**, Kaul, A., Bakir, M., & Raychowdhury, A. (2020). A Model Study of Multilevel Signalling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration, In *Proceedings of 28th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2020)*, Salt Lake City, USA.
11. **Saligram**, **R.**, Abhilash, P., & Patel, K. (2018). Realization of Multivalued Logic Combinational Circuits in Fully Depleted Silicon on Insulator, In *Proceedings of IEEE International Conference on Networking, Embedded and Wireless Systems*, Bangalore.
12. **Saligram**, **R.**, Jyoti, K., & Patel, K. (2018). Quarternary digital circuits design using carbon nanotube fets, In *Proceedings of IEEE International Conference on Networking, Embedded and Wireless Systems*, Bangalore.
13. Bairy, B., Craig, T. S., Gonde, K., Gupta, N., Prajogi, A., Wilner, M., & **Saligram**, **R.** (2016a). Towards mitigating the impact of NBTI and PBTI Degradation, In *Proceedings of 2nd World Congress on Automation and Robotics Conference*, Pennsylvania.

14. **Saligram**, **R.** (2013a). Design and Implementation of Logical Cost Efficient Nanometric Fault Tolerant Reversible BCD Adder, In *Proceedings of IEEE 10th INDICON*, IIT Bombay.

15. **Saligram**, **R.** (2013b). Design of Low Logical Cost Conservative Reversible Adders using Novel PCTG, In *Proceedings of IEEE 4th International Symposium on Electronic System Design*, Singapore.

16. **Saligram**, **R.**, & Ravishankar, R. (2013a). Design of Low Logical Cost Adders using Novel Parity Conserving Toffoli Gate, In *Proceedings of IEEE International Conference on Emerging Trends in Communication, Control, Signal Processing and Computing Applications*.

17. Ravishankar, R., & **Saligram**, **R.** (2013a). Design of high speed low power multiplier using reversible logic: A vedic mathematical approach, In *Proceedings of IEEE International Conference on Circuits Power and Computing Technologies*.

18. Ravishankar, R., & **Saligram**, **R.** (2013b). Parity preserving logic based fault tolerant reversible ALU, In *Proceedings of IEEE International Conference on Information and Communication Technologies*.

19. **Saligram**, **R.**, & Ravishankar, R. (2013b). Contemplation of synchronous gray code counter and its variants using reversible logic gates, In *Proceedings of IEEE International Conference on Information and Communication Technologies*.

20. **Saligram**, **R.**, & Ravishankar, R. (2013c). Optimized reversible vedic multipliers for high speed low power operations, In *Proceedings of IEEE International Conference on Information and Communication Technologies*.

21. **Saligram**, **R.**, & Ravishankar, R. (2013d). Towards the Design of Fault Tolerant Reversible Circuits Components of ALU using New PCMF Gate, In *Proceedings of IEEE International Conference on Advances in Computing, Communication and Informatics*.

Books and Chapters

1. **Saligram**, **R.**, Kaul, A., Bakir, M. S., & Raychowdhury, A. (2021). Multilevel Signalling for High-Speed Chiplet-to-Chiplet Communication, In *VLSI-SoC New Technology Enabler*. Springer.

2. Chen, Z., Gonde, K., Ravicz, K., **Saligram**, **R.**, Schlesinger, M., & Wilner, M. (2016). Concluding remarks, In *Wireless Computing in Medicine: From Nano to Cloud with Ethical and Legal Implications*. Wiley.

Talks

Invited

2023 **Cryogenic CMOS for Quantum Computing**, *GT ECE Quantum Computing Devices and Hardware-Guest Lecture*

2022 **Cryogenic CMOS for High Performance Computing**, *Microsoft Corp.*

2020 **Cryogenic CMOS VLSI Circuits**, *ARM Inc.*

2019 **Modelling of High-Speed Channels**, *Liaison Meeting at Semiconductor Research Corporation*

Skills

EDA	Synopsys Design Compiler, Prime Time, IC-Compiler (ICC/ICC2), Lynx, Cadence NC Sim, Genus, Innovus, Encounter, Virtuoso, Mentor Graphics Modelsim, Calibre
Modelling	Synopsys TCAD Sentaurus, Ansys HFSS, Keysight ADS.
Scripting	Tcl, Perl
HDL	Verilog, VDHL
OS	Windows, RHEL, Ubuntu, Mac

Awards and Recognition

Corporate

2018
- **Team Recognition**, *by Section Execution Owner for Pioneering partition execution to foster clear & realistic utilization targets.*
- **Team Recognition**, *by Section Execution Owner for achieving LV closure on two partitions through contingency support.*

2017
- **Team Recognition**, *by Section Execution Owner for Pioneering partition LV release for DSSM Section Aostepping.*
- **SQO Recognition**, *by Caliber COE for discovering Innovative methods for fixing Max-Cap Violations on RP-cells with no degradation in other metrics.*
- **SQO Recognition**, *by Full Chip Caliber Owner for flagging and Pioneering Caliber Issues at FC level and DSSM Section Level.*
- **Team Recognition**, *by Section Execution Owner for supporting multiple section PV to clean up timing violations due to standard cell library changes and for Supporting multiple iterations of Black-box FC-ILM PV to converge inter section paths.*
- **Team Recognition**, *by Section Execution Owner for hacking central SD RTL models to match SSM Floorplan hierarchy and releasing central synthesis netlist, section Bitblast netlist for Floor planning*
- **Team Recognition**, *by Section Execution Owner appreciating efforts in flagging and resolving routing issues with 10nm++ additional metal stacks in ICC2 with Gen11 and Gen12 RTL*

2016
- **Team Recognition**, *by Section Execution Owner for efforts in launching multiple section PV and Caliber*

Academic

2022
- **Finalists, Qualcomm Innovation Fellowship**, *Privacy Preserving Computing for Edge Devices using Energy Efficient Homomorphic Encryption Accelerators*

2020
- **GT-ORNL PhD Seed Research Grant Award**, *Cryogenic CMOS interface circuits for superconducting quantum circuits.*

2016
- **MS Honors**, *USC Ming Hsieh Institute-Department of Electrical Engineering.*

2012
- **Best paper award at IEEE International Conference on Circuits Power and Computing Technologies**, *Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach*

2009-13
- **Ministry of Human Resource Development (MHRD) Scholarship**, *Sponsored by the Government of India*

2009
- **Gnana Shree State Award & Vidya Ratna Puraskar**, *10th Rank in Karnataka State Pre-University, Bangalore, India*

Professional Services

Reviewer

2023
- **IEEE Transactions on VLSI**, July
- **IEEE Solid State Circuit Letters**, June
- **IEEE Electron Device Letters**, May, June
- **IEEE Transactions on Circuits and Systems-II: Express Briefs**, April

2022
- **IEEE Transactions on VLSI**, December
- **IEEE Electron Device Letters**, April, September

2017
- **IEEE Transactions on VLSI**, September

Professional Services (continued)

2016 **Microelectronics Journal Elsevier**, November

Alexandria Engineering Journal, July

2015 **ACM Journal on Emerging Technology in Computing**, August

Microelectronics Journal Elsevier, July

Microelectronics Journal Elsevier, January

Organization

2022 **GT-IMEC Meeting**, to discuss collaboration opportunities for superconducting computers.

2014 **Digital Front End Design and Implementation using Synopsys Tools**, Two Week Faculty Development Program.

Antenna Technologies, One week Faculty Development Workshop.